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(71) Applicant: CANON KABUSHIKI KAISHA
Tokyo (JP)

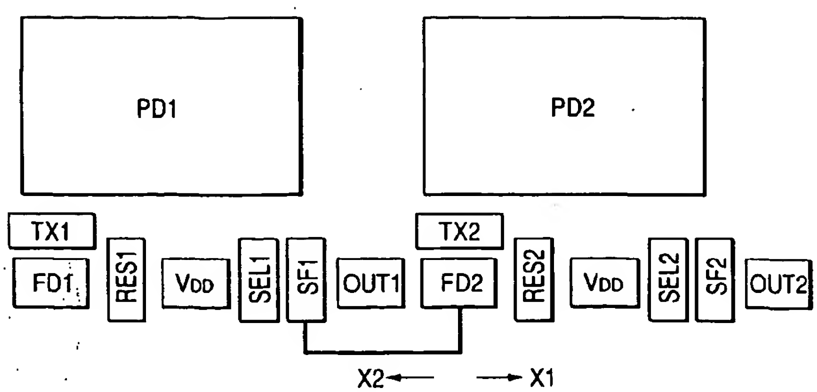
(72) Inventors:
- Sakurai, Katsuhito, Canon Kabushiki Kaisha Tokyo (JP)
- Ogawa, Katsuhisa, Canon Kabushiki Kaisha Tokyo (JP)
- Sugawa, Shigetoshi, Canon Kabushiki Kaisha Tokyo (JP)
- Koizumi, Toru, Canon Kabushiki Kaisha Tokyo (JP)
- Kochi, Tetsunobu, Canon Kabushiki Kaisha Tokyo (JP)
- Ueno, Isamu, Canon Kabushiki Kaisha Tokyo (JP)
- Hiyama, Hiroki, Canon Kabushiki Kaisha Tokyo (JP)

(74) Representative:
Beresford, Keith Denis Lewis et al
BERESFORD & Co.
2-5 Warwick Court
High Holborn
London WC1R 5DJ (GB)

(54) **Solid-state image pickup device**

(57) To optimize the layout of a pixel portion, there is provided a solid-state image pickup device including a photoelectric conversion portion, a charge transfer portion for transferring signal charges generated in the photoelectric conversion portion, and an amplifier portion for amplifying a signal corresponding to the signal charges transferred from the charge transfer portion and outputting the signal, wherein a plurality of photoelectric conversion portions, a plurality of charge transfer portions, and a plurality of amplifier portions are arranged in the row or/and column directions, and the charge transfer portion and the amplifier portion which are closest to each other are connected.

FIG. 4



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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a solid-state image pickup device and an image pickup system using the same and, more particularly, to a solid-state image pickup device having a plurality of photoelectric conversion portions arrayed in the row and column directions, a charge transfer means for transferring signal charges generated in the photoelectric conversion portions, and an amplifier means for amplifying a signal corresponding to the signal charges transferred by the charge transfer means and outputting the signal.

Related Background Art

[0002] There are conventional solid-state image pickup devices which use photodiodes as photoelectric conversion portions and move photocarriers stored in the photodiodes using a FET or CCD. These solid-state image pickup devices are used for various apparatuses such as solar cells, image cameras, copying machines, and facsimile apparatuses and also improving in their conversion efficiency and integration density.

[0003] A device of FET moving scheme is known as a MOS solid-state image pickup device. For example, a solid-state image pickup device called a CMOS sensor is disclosed in Japanese Laid-Open Patent Application No. 09-46596. The arrangement will be briefly described below.

[0004] Fig. 1 is an explanatory view showing a pixel arrangement corresponding to one pixel of a CMOS sensor disclosed in Fig. 8 of Japanese Laid-Open Patent Application No. 09-46596.

[0005] As shown in Fig. 1, one pixel has a photodiode portion PD, a transfer switch MS11 for transferring signal charges from the photodiode portion PD, an amplifier means MS14 for amplifying the transferred signal and outputting it, a selection switch MS13 for selecting the pixel, and a reset switch MS12 for clearing the remaining signal charges and resetting them to a potential VR. Signals ϕTX, ϕRES, and ϕSEL are used to control the transfer switch MS11, reset switch MS12, and selection switch MS13, respectively.

[0006] For the above solid-state image pickup device, an optimum layout of building members (transfer switch, amplifier means, selection switch, and reset switch) of a pixel is not disclosed. According to the study by the present inventors, in certain arrangements of pixel building members or interconnections, crosstalk from the signal ϕRES or ϕSEL poses a problem, the fill factor lowers due to interconnections, or the sensitivity lowers due to an increased capacitance in the presence of interconnections.

SUMMARY OF THE INVENTION

[0007] It is an object of the present invention to provide an optimum layout of building components around a photoelectric conversion portion.

[0008] In order to achieve the above object, according to an aspect of the present invention, there is provided a solid-state image pickup device comprising a photoelectric conversion portion, charge transfer means for transferring signal charges generated in the photoelectric conversion portion, and amplifier means for amplifying a signal corresponding to the signal charges transferred from the charge transfer means and outputting the signal, wherein a plurality of photoelectric conversion portions, a plurality of charge transfer means, and a plurality of amplifier means are arranged in row or/and column directions, and the charge transfer means and the amplifier means which are closest to each other are connected.

[0009] According to another aspect of the present invention, there is provided a solid-state image pickup device wherein a plurality of photoelectric conversion portions are arranged in row and column directions, and charge transfer means for transferring signal charges generated in the photoelectric conversion portions are arranged in the row and column directions in correspondence with the photoelectric conversion portions, and reset means for resetting the charge transfer means or the charge transfer means and the photoelectric conversion portions corresponding to the charge transfer means are arranged on one side of an array direction of the charge transfer means, and amplifier means for amplifying a signal corresponding to the signal charges transferred from the charge transfer means are arranged on the other side of the array direction of the charge transfer means.

[0010] According to still another aspect of the present invention, there is provided a solid-state image pickup device wherein a plurality of photoelectric conversion portions are arranged in row and column directions, and charge transfer means for transferring signal charges generated in the photoelectric conversion portions and reset means for resetting the charge transfer means or the charge transfer means and the photoelectric conversion portions are arranged in one of the row and column directions around the photoelectric conversion portions, and amplifier means for amplifying a signal corresponding to the signal charges transferred from one photoelectric conversion portion and outputting the signal is arranged in the other direction different from the one direction of the one photoelectric conversion portion around which the charge transfer means and the reset means are arranged or in the other direction around another photoelectric conversion portion in a diagonal direction, the amplifier means being arranged on a side closest to the one photoelectric conversion portion.

[0011] According to still another aspect of the present invention, there is provided an image pickup system

comprising a solid-state image pickup device including a photoelectric conversion portion, charge transfer means for transferring signal charges generated in the photoelectric conversion portion, and amplifier means for amplifying a signal corresponding to the signal charges transferred from the charge transfer means and outputting the signal, wherein a plurality of photoelectric conversion portions, a plurality of charge transfer means, and a plurality of amplifier means are arranged in row or/and column directions, and the charge transfer means and the amplifier means which are closest to each other are connected, and a signal processing circuit for processing the signal output from the solid-state image pickup device.

[0012] With the above arrangement, a high fill factor and high sensitivity can be obtained.

[0013] Other objects, features, and advantages of the invention will be apparent from the following specification and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014]

Fig. 1 is a view showing one pixel of a solid-state image pickup device;

Fig. 2 is a view showing a schematic layout of a solid-state image pickup device;

Fig. 3 is a view showing another schematic layout of a solid-state image pickup device;

Fig. 4 is a view showing a schematic layout of a solid-state image pickup device according to the first embodiment;

Fig. 5 is a view showing a specific layout of the solid-state image pickup device according to the first embodiment;

Fig. 6 is a view showing the specific layout of the solid-state image pickup device according to the first embodiment;

Fig. 7 is a view showing a schematic layout of a solid-state image pickup device according to the second embodiment;

Fig. 8 is a view showing a modification of the schematic layout of the solid-state image pickup device according to the second embodiment;

Fig. 9 is a view showing another modification of the schematic layout of the solid-state image pickup device according to the second embodiment;

Fig. 10 is a view showing still another modification of the schematic layout of the solid-state image pickup device according to the second embodiment;

Fig. 11 is a view showing still another modification of the schematic layout of the solid-state image pickup device according to the second embodiment;

Fig. 12 is a view showing a specific layout of the solid-state image pickup device according to the second embodiment;

Fig. 13 is a view showing the specific layout of the solid-state image pickup device according to the second embodiment;

Fig. 14 is a view showing the circuit arrangement of a pixel portion of the solid-state image pickup devices of the first and second embodiments;

Fig. 15 is a view showing another pixel of the solid-state image pickup device;

Fig. 16 is a view showing a schematic layout of a solid-state image pickup device according to the third embodiment; and

Fig. 17 is a view showing an image pickup system using one of the solid-state image pickup devices of the first to third embodiments.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0015] The embodiments of the present invention will be described below. Before the description, the technical backgrounds of the present invention will be described.

[0016] As the arrangement of one pixel of an solid-state image pickup device, an arrangement having a photodiode portion (PD), a transfer switch (TX), a floating diffusion (FD), a reset switch (RES), a reset power source (VR), a selection switch (SEL), an amplifier means (SF), an output portion (OUT), and a VDD power source (VDD) will be described.

[0017] In this solid-state image pickup device, to increase the area of the photodiode portions (PD) for storing charges after photoelectric conversion in the arrayed pixels, building members other than the photodiode portions (PD) must be mounted around the photodiode portions (PD) at high density. To increase the fill factor of the pixels, preferably the number of contacts is decreased and all pixels have equal diffusion regions.

[0018] From the above viewpoint, when a VDD power source is used as a reset power source, an arrangement shown in Fig. 2 is preferably used. If the reset power source (VR) is arranged independently of the VDD power source, an arrangement shown in Fig. 3 is preferably used.

[0019] However, when the floating diffusion FD and the gate of the amplifier means (SF) are connected, the arrangement shown in Fig. 2 or 3 has the following disadvantages.

(1) In the arrangement shown in Fig. 2 or 3, the control line of a signal ϕTX for controlling the transfer switch (TX), the control line of a signal ϕRES for controlling the reset switch (RES), and the control line of a signal ϕSEL for controlling the selection switch (SEL) extend in the horizontal direction (column direction) between adjacent photodiode portions PD.

To connect the floating diffusion (FD) and the

gate of the amplifier means (SF) without increasing the interval between the photodiode portions PD where the control lines extend, the floating diffusion and the gate of the amplifier means are connected by a multilayered interconnection running above the gate of the reset switch (RES) or the gate of the selection switch (SEL).

In this case, however, crosstalk from the signal ϕRES or ϕSEL to the floating diffusion (FD) poses a problem.

(2) When an interconnection is to be formed while avoiding the gate of the reset switch RES or selection switch SEL, it must be formed on the photodiode portions PD, which lowers the fill factor.

(3) If the interconnection between the floating diffusion (FD) and the gate of the amplifier means (SF) is long, the FD capacitance increases to lower the sensitivity.

[0020] The present invention has been made as a result of extensive studies and examinations by the present inventors to solve the above problem while maintaining the arrangement shown in Fig. 2 or 3.

[0021] The embodiments of the present invention will be described below.

[0022] Throughout the drawings to be described below, suffices added to PD, TX, SEL, OUT, RES, SF, and FD indicate not members for transferring, outputting, and resetting signals from one photodiode portion PD but members arranged around one photodiode portion PD which will be normally recognized to be one pixel.

[0023] The layout of a sensor of this type is shown in, e.g., Figs. 6 and 9 (CMOS sensor using a photogate) or Fig. 10 (CMOS sensor using a photodiode) in "CMOS Active Pixel Image Sensors for Highly Integrated Imaging Systems", IEEE Journal of Solid-State Circuits, Vol. 32, No. 2, February 1997, pp. 187 - 197. One pixel of a sensor of this type normally has an almost rectangular shape or a shape similar to a rectangle, and pixel building members including a transfer switch TX and a reset switch RES are located around the photoelectric conversion portion such as a photodiode portion PD. Hence, in the present invention, an arrangement having a photodiode portion PD2, a transfer switch TX2, a floating diffusion FD2, a reset switch RES2, a selection switch SEL2, an amplifier means SF2, and an output portion OUT2, as shown in Fig. 4, 5, 7, or 12 etc., may be regarded as one pixel, so a signal may be output from the pixel having the photodiode portion PD2 using an amplifier means SF1 or SF3 of another pixel.

[0024] Fig. 4 is a view showing a schematic layout of the first embodiment of the present invention. This embodiment corresponds to the arrangement shown in Fig. 2 which uses a VDD power source as a reset power source. In this embodiment, as shown in Fig. 4, to read out a signal from the photodiode portion PD2 using an amplifier means SF1 and an output portion OUT1 on the adjacent photodiode portion PD1 side, the floating diffusion FD2 around the photodiode portion PD2 is connected to the amplifier means SF1 on the photodiode portion PD1 side.

[0025] In this arrangement, the interconnection is shorter than that when the floating diffusion FD2 and the gate of the amplifier means SF2 are connected, and the interconnection does not run above the gate of the reset switch RES2 or the gate of the selection switch SEL2. Consequently, problems (1) to (3) above can be solved.

[0026] Figs. 5 and 6 are views showing the schematic layout shown in Fig. 4 more specifically. Fig. 5 shows a layout without a second aluminum layer as an upper interconnection. Fig. 6 shows a layout including a second aluminum layer as an upper interconnection. Figs. 5 and 6 show only four pixels. Only a signal read from the photodiode portion PD2 will be described below, and this also applies to the remaining photodiode portions.

[0027] As shown in Fig. 5, the transfer switch TX2, floating diffusion FD2, reset switch RES2, selection switch SEL2, amplifier means SF2, and output portion OUT2 surround around the photodiode portion PD2. A VDD power source which also serves as a reset power source is interposed between the reset switch RES2 and the selection switch SEL2. A region indicated by a bold line in Fig. 5 is an active region.

[0028] In this embodiment, the signal from the photodiode portion PD2 is output not through the amplifier means SF2 and output portion OUT2 but through the amplifier means SF1 and output portion OUT1 arranged on the side of the photodiode portion PD1 arrayed on the same row. For this purpose, the floating diffusion FD2 on the photodiode portion PD2 side and the amplifier means SF1 on the photodiode portion PD1 side are connected using a polysilicon layer and a first aluminum layer. The amplifier means SF1 and output portion OUT1 are formed in the same active region as that of the photodiode portion PD1.

[0029] According to this embodiment, the interconnection between the floating diffusion FD and the amplifier means SF shortens, and the interconnection is not formed above the gate of the reset switch RES or the gate of the selection switch SEL. In addition, in this embodiment, the interconnection between the floating diffusion FD2 and the amplifier means SF1 runs between the control line of a signal ϕnSEL and the control line of a signal ϕnRES to prevent the output signal from being influenced by the signal ϕnSEL or ϕnRES, as shown in Fig. 6.

[0030] Fig. 7 is a view showing a schematic layout of the second embodiment of the present invention. This embodiment corresponds to the arrangement shown in Fig. 3 having a reset power source independently of a VDD power source. As shown in Fig. 7, in this embodiment, to output a signal from a photodiode portion PD2 using an amplifier means (SF3) and output portion (OUT3) surrounding a photodiode portion PD3 in the diagonal direction, a floating diffusion FD2 around the photodiode portion PD2 is connected to the amplifier

means SF3 around the photodiode portion PD3.

[0031] In this arrangement, the interconnection shortens and does not run above the gate of a reset switch RES2, so problems (1) to (3) above can be solved, as in the first embodiment.

[0032] In addition, according to this embodiment, even when the interconnection is formed on the control line of a signal ϕSEL using a multilayered interconnection, no crosstalk is generated. More specifically, in this embodiment, even when the control line of the signal ϕSEL for controlling a selection switch (SEL) extends above the floating diffusion FD2, the control line is connected to not the selection switch SEL3 but the selection switch SEL2 on the next, upper row (a select pulse signal is not applied to the selection switch SEL2), so no crosstalk is generated.

[0033] Various modifications as will described below can be made for the second embodiment.

(I) As shown in Fig. 8, the amplifier means SF and selection switch SEL are reversed.

(II) As shown in Fig. 9, the transfer switch TX2, floating diffusion FD2, reset switch RES2, and reset power source VR are mounted on the upper side of the photodiode portion PD2, and the floating diffusion FD2 is connected to the amplifier means SF (not shown) on the upper row.

(III) As shown in Fig. 10, the selection switch SEL, output portion OUT, VDD power source VDD, and amplifier means SF are located on the left side of the photodiode portion PD.

(IV) As shown in Fig. 11, the floating diffusion FD is located on the right side of the drawing, the arrangement of the transfer switch TX, floating diffusion FD, reset switch RES, and reset power source VR is reversed to that in Fig. 7, and the floating diffusion FD is connected to the photodiode portion PD on the lower side.

[0034] In the above-described drawings, the photodiode portion PD has a rectangular shape. However, the photodiode portion PD need not always have this shape and can have any shape as far as the shape allows to maximize the amount of charges to be stored.

[0035] Figs. 12 and 13 are views showing the layout in Fig. 7 more specifically. Fig. 12 shows a layout without a second aluminum layer as an upper interconnection. Fig. 13 shows a layout including a second aluminum layer as an upper interconnection. Figs. 12 and 13 show only four pixels. Only a signal read from the photodiode portion PD2 will be described below, and this also applies to the remaining photodiode portions.

[0036] As shown in Fig. 12, the transfer switch TX2, floating diffusion FD2, reset switch RES2, selection switch SEL2, amplifier means SF2, and output portion OUT2 are arranged around the photodiode portion PD2. A reset power source Vr and VDD power source are mounted adjacent to the reset switch RES2 and selection switch SEL2. Two regions indicated by bold lines in Fig. 12 are active regions.

[0037] In this embodiment, the signal from the photodiode portion PD2 is output not through the amplifier means SF2 and output portion OUT2 but through the amplifier means SF3 and output portion OUT3 surrounding the photodiode portion PD3 in the diagonal direction. For this purpose, the floating diffusion FD2 around the photodiode portion PD2 and the amplifier means SF3 around the photodiode portion PD3 are connected using a polysilicon layer and a first aluminum layer.

[0038] According to this embodiment, the interconnection between the floating diffusion FD and the amplifier means SF shortens, and the interconnection does not run above the gate of the reset switch RES or the gate of the selection switch SEL.

[0039] In this embodiment, the gate of the selection switch SEL3 is connected to the control line of the signal ϕnSEL. For this reason, even when the control line of a signal ϕn+1SEL extends above the floating diffusion FD2, the problem of crosstalk is not posed.

[0040] Fig. 14 is a view showing the circuit arrangement of a pixel portion of the solid-state image pickup devices of the first and second embodiments.

[0041] Fig. 14 shows a 4 × 4 pixel arrangement, and one pixel has the same arrangement as that shown in Fig. 1.

[0042] The present invention is not limited to the pixel arrangement shown in Fig. 1. As the third embodiment, a selection means may be connected between an amplifier means and an output portion, as shown in Fig. 15.

[0043] Fig. 16 is a view showing a schematic layout of a solid-state image pickup device having the pixel arrangement shown in Fig. 15.

[0044] In the layout shown in Fig. 16, a VDD power source VDD and output portion OUT are reversed to those of the layout shown in Fig. 2. With this layout, the interconnection becomes shorter than that in connecting a floating diffusion FD2 and the gate of an amplifier means SF2, so the interconnection does not run above the gate of a reset switch RES2 and the gate of a selection switch SEL2.

[0045] Fig. 17 is a view schematically showing, as the fourth embodiment, a solid-image pickup system using one of the solid-state image pickup devices described in the first to third embodiments. As shown in Fig. 17, the image of light incident through an optical system 71 and an iris 80 is formed on a solid-state image pickup device 72. The light information is converted into an electrical signal by a pixel array on the solid-state image pickup device 72 and output. The output signal is converted by a signal processing circuit 73 on the basis of a predetermined scheme and output. The processed signal is recorded or transferred by an information recording device in a recording system/communication system 74. The recorded or transferred signal is reproduced by a reproducing system 77. The iris 80, solid-

state image pickup device 72, and signal processing circuit 73 are controlled by a timing control circuit 75. The optical system 71, timing control circuit 75, recording system/communication system 74, and reproducing system 77 are controlled by a system control circuit 76.

[0046] As has been described above, according to the first to fourth embodiments, the interconnection between the floating diffusion (FD) and the amplifier means (SF) shortens, and the interconnection does not run above the gate of the reset means (RES) and the gate of the selection means (SEL). Since no crosstalk is generated from the signal ϕRES or ϕSEL, a solid-state image pickup device having a high fill factor and sensitivity and an image pickup system using the device can be obtained.

[0047] Many widely different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention. It should be understood that the present invention is not limited to the specific embodiments described in the specification, except as defined in the appended claims.

Claims

1. A solid-state image pickup device comprising:

    a photoelectric conversion portion;
    charge transfer means for transferring signal charges generated in said photoelectric conversion portion; and
    amplifier means for amplifying a signal corresponding to the signal charges transferred from said charge transfer means and outputting the signal,
    wherein a plurality of photoelectric conversion portions, a plurality of charge transfer means, and a plurality of amplifier means are arranged in row or/and column directions, and
    said charge transfer means and said amplifier means which are closest to each other are connected.

2. A solid-state image pickup device comprising: a plurality of photoelectric conversion portions arranged in row and column directions;

    charge transfer means for transferring signal charges generated in said photoelectric conversion portions, said charge transfer means being arranged in the row and column directions in correspondence with said photoelectric conversion portions;
    reset means for resetting said charge transfer means or said charge transfer means and said photoelectric conversion portions corresponding to said charge transfer means, said reset means being arranged on one side of an array direction of said charge transfer means; and
    amplifier means for amplifying a signal corresponding to the signal charges transferred from said charge transfer means, said amplifier means being arranged on the other side of the array direction of said charge transfer means.

3. A device according to claim 2, wherein said photoelectric conversion portion and said charge transfer means are formed in an active region, and said amplifier means is formed in another active region including another photoelectric conversion portion adjacent to said photoelectric conversion portion.

4. A device according to claim 2, wherein selection means for selecting said amplifier means to supply a voltage are arranged to be adjacent to said amplifier means on the other side of the array direction of said charge transfer means, and the voltage and a reset voltage to be supplied to said reset means are supplied from a common power source.

5. A device according to claim 3, wherein selection means for selecting said amplifier means to supply a voltage are arranged to be adjacent to said amplifier means on the other side of the array direction of said charge transfer means, and the voltage and a reset voltage to be supplied to said reset means are supplied from a common power source.

6. A solid-state image pickup device comprising: a plurality of photoelectric conversion portions arranged in row and column directions;

    charge transfer means for transferring signal charges generated in said photoelectric conversion portions; and
    reset means for resetting said charge transfer means or said charge transfer means and said photoelectric conversion portions, said charge transfer means and said reset means being arranged in one of the row and column directions around said photoelectric conversion portions; and
    amplifier means for amplifying a signal corresponding to the signal charges transferred from one photoelectric conversion portion and outputting the signal, said amplifier means being arranged in the other direction different from the one direction of said one photoelectric conversion portion around which said charge transfer means and said reset means are arranged or in the other direction around another photoelectric conversion portion in a diagonal direction, wherein said amplifier means is arranged on a side closest to said one photoelectric conversion portion.

7. A device according to claim 6, further comprising selection means, arranged adjacent to said amplifier means of each photoelectric conversion portion, for selecting said amplifier means to supply a voltage, and

between one photoelectric conversion portion array in the one direction including said one photoelectric conversion portion and another photoelectric conversion portion array in the one direction including said other photoelectric conversion portion, a first control line for controlling each charge transfer means of said one photoelectric conversion portion array, a second control line for controlling each reset means, and a third control line for controlling said selection means of photoelectric conversion portion arrays other than said one photoelectric conversion portion array are arranged.

8. An image pickup system comprising:

(A) a solid-state image pickup device including:

(a) a photoelectric conversion portion;
(b) charge transfer means for transferring signal charges generated in said photoelectric conversion portion; and
(c) amplifier means for amplifying a signal corresponding to the signal charges transferred from said charge transfer means and outputting the signal,

wherein a plurality of photoelectric conversion portions, a plurality of charge transfer means, and a plurality of amplifier means are arranged in row or/and column directions, and said charge transfer means and said amplifier means which are closest to each other are connected, and
(B) a signal processing circuit for processing the signal output from said solid-state image pickup device.

FIG. 1

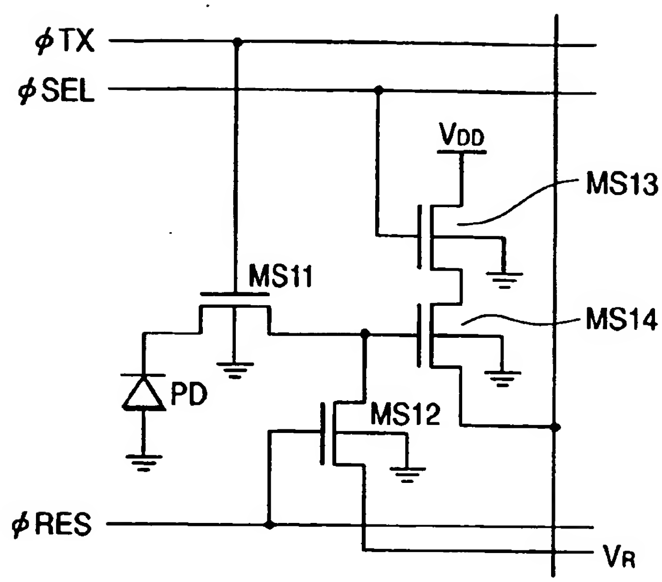

φTX
φSEL
VDD
MS13
MS11
MS14
PD
MS12
φRES
VR

FIG. 2

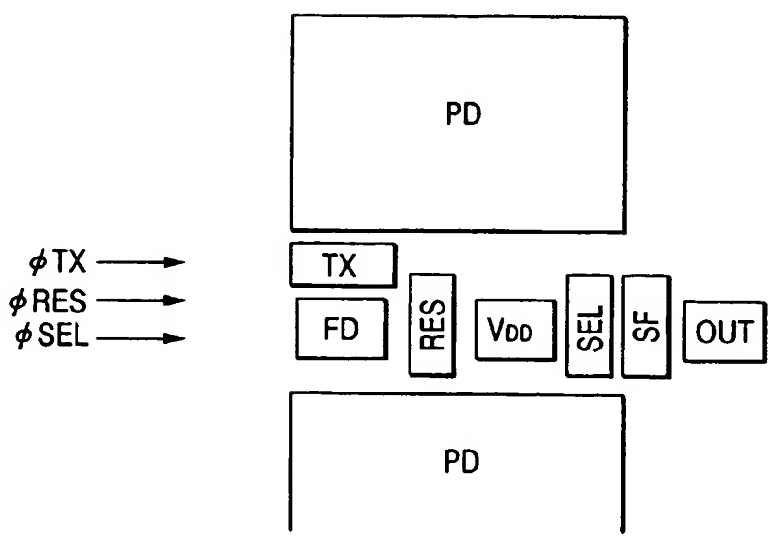

PD
φTX
φRES
φSEL
TX
FD
RES
VDD
SEL
SF
OUT
PD

FIG. 3

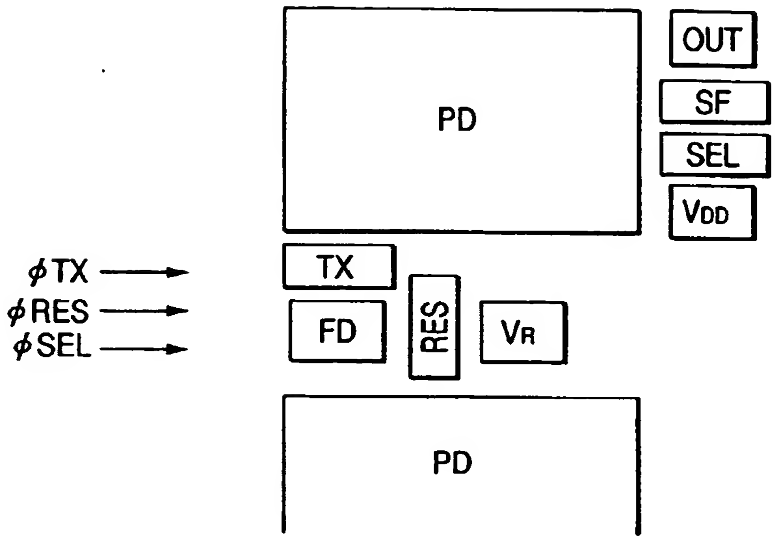

OUT
SF
SEL
VDD
PD
ϕTX
ϕRES
ϕSEL
TX
FD
RES
VR
PD

FIG. 4

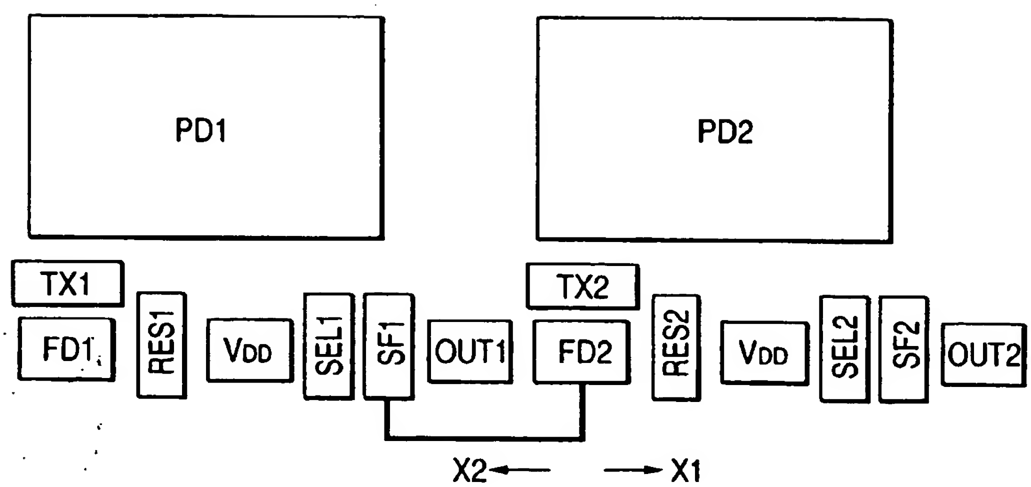

PD1
PD2
TX1
FD1
RES1
VDD
SEL1
SF1
OUT1
TX2
FD2
RES2
VDD
SEL2
SF2
OUT2
X2
X1

FIG. 5

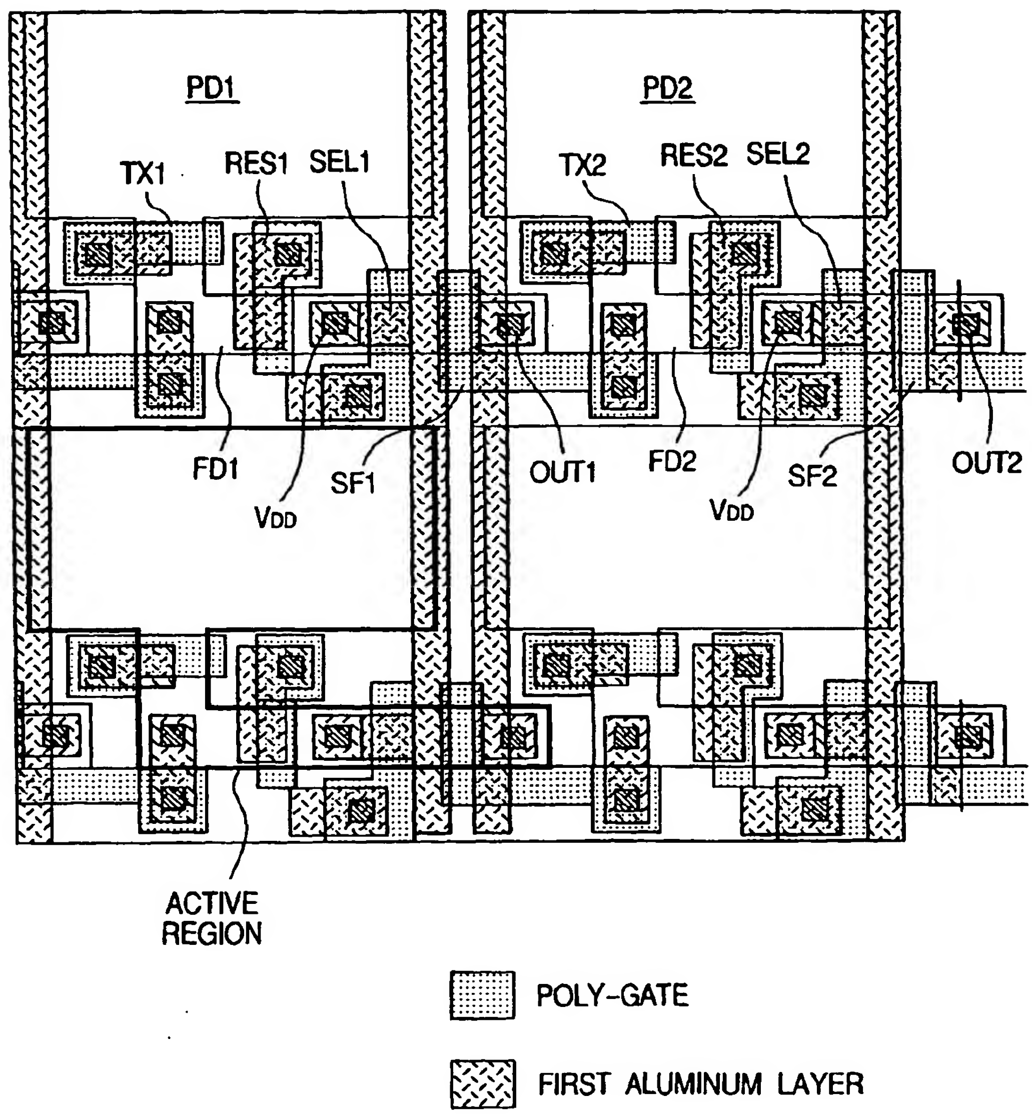

PD1
PD2
TX1
RES1
SEL1
TX2
RES2
SEL2
FD1
VDD
SF1
OUT1
FD2
VDD
SF2
OUT2
ACTIVE REGION
POLY-GATE
FIRST ALUMINUM LAYER

FIG. 6

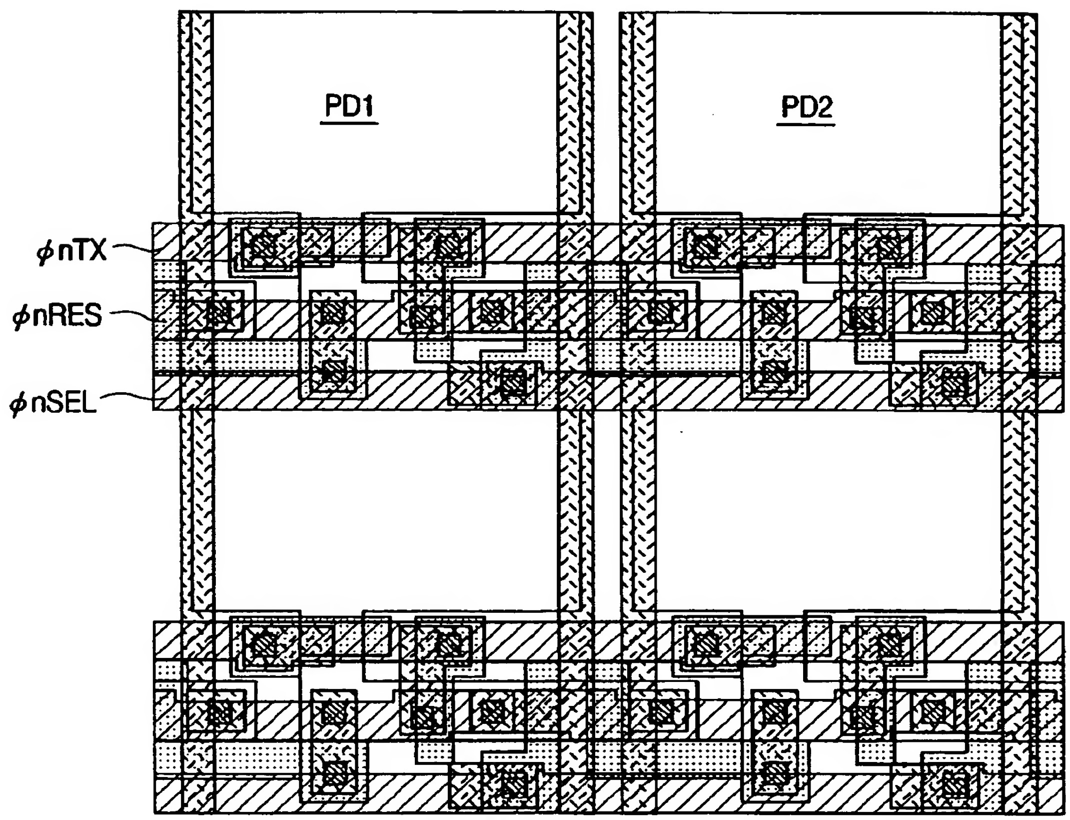


FIG. 7

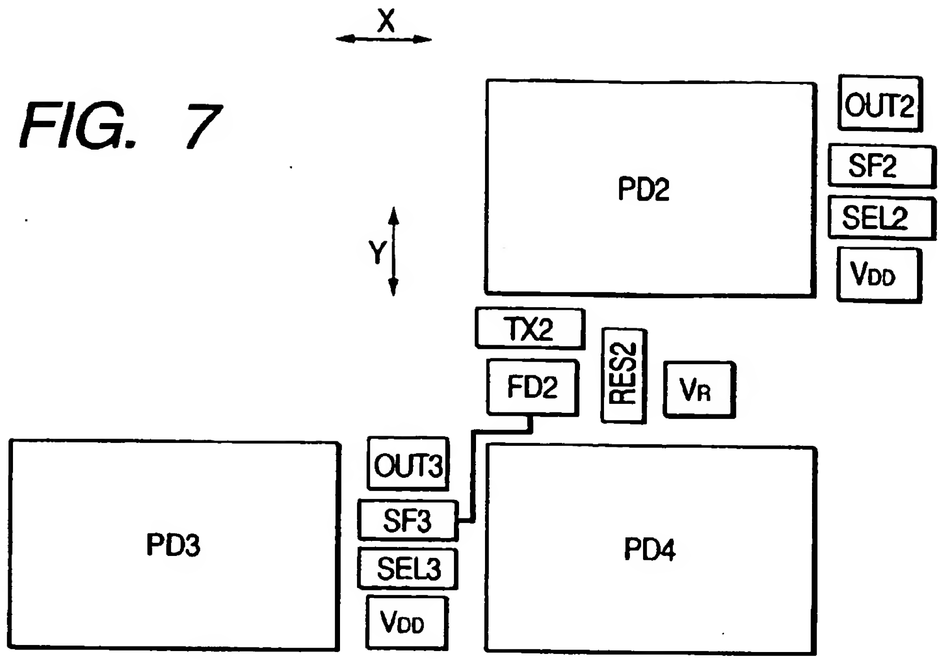

X
Y
PD2
OUT2
SF2
SEL2
VDD
TX2
FD2
RES2
VR
PD3
OUT3
SF3
SEL3
VDD
PD4

FIG. 8

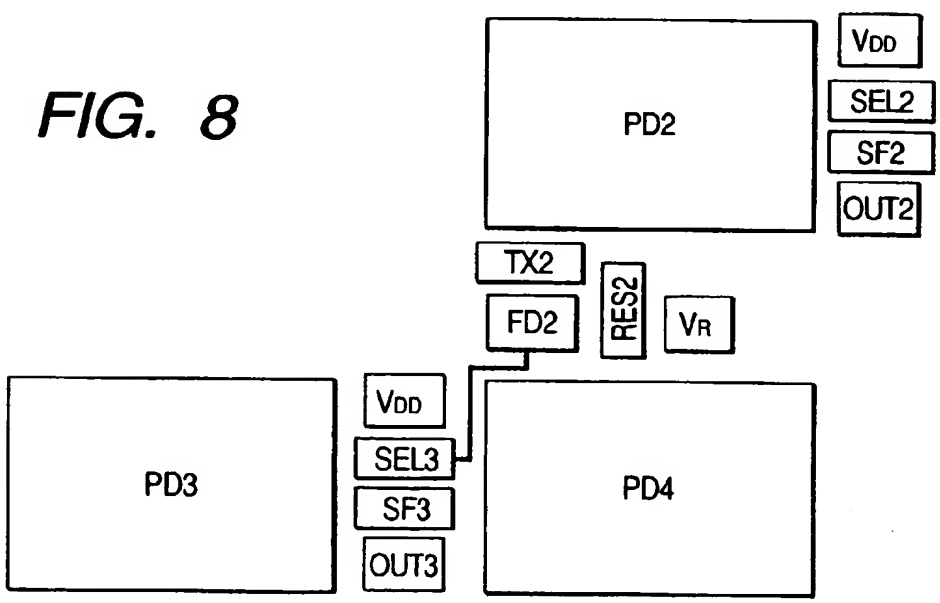

PD2
VDD
SEL2
SF2
OUT2
TX2
FD2
RES2
VR
PD3
VDD
SEL3
SF3
OUT3
PD4

FIG. 9

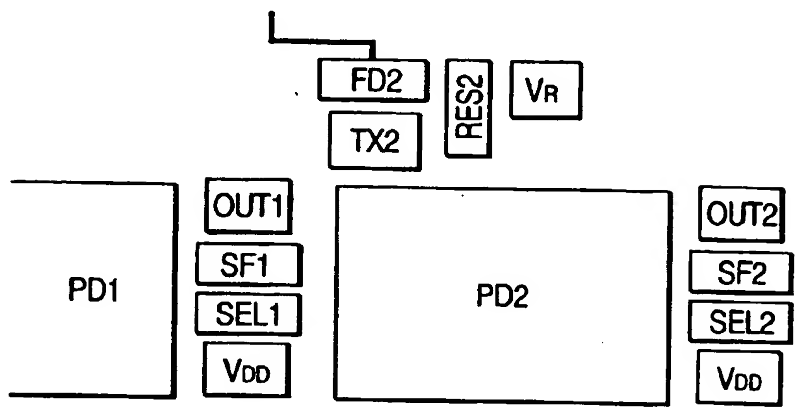

FD2
RES2
VR
TX2
OUT1
SF1
SEL1
VDD
PD1
PD2
OUT2
SF2
SEL2
VDD

FIG. 10

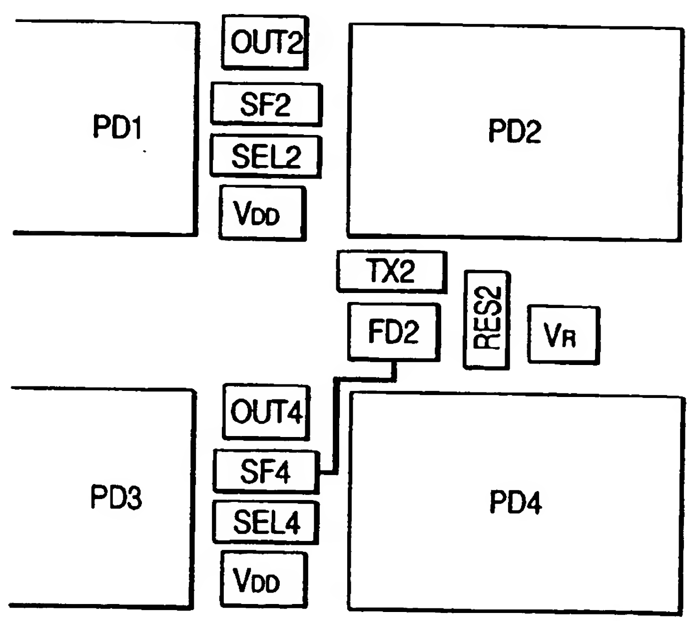

OUT2
SF2
SEL2
VDD
PD1
PD2
TX2
FD2
RES2
VR
OUT4
SF4
SEL4
VDD
PD3
PD4

FIG. 11

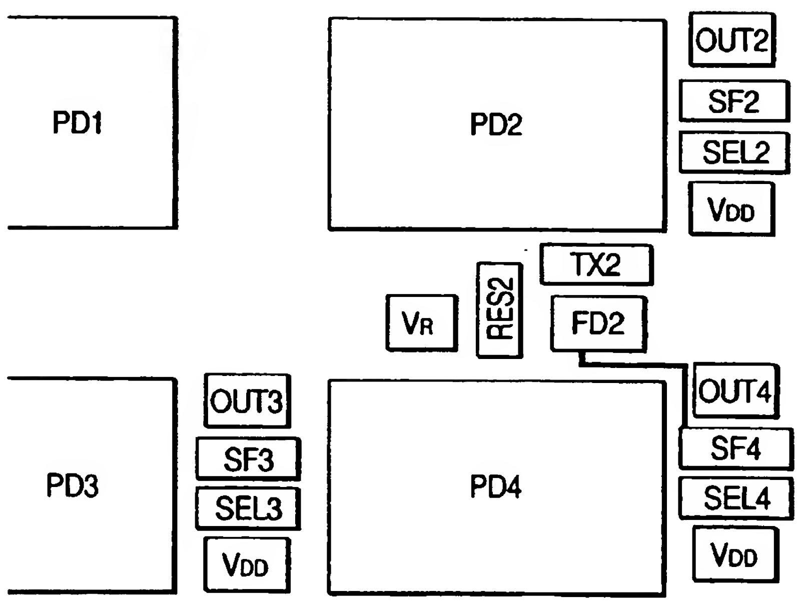

PD1
PD2
OUT2
SF2
SEL2
VDD
TX2
RES2
VR
FD2
OUT4
SF4
SEL4
VDD
PD3
OUT3
SF3
SEL3
VDD
PD4

FIG. 12

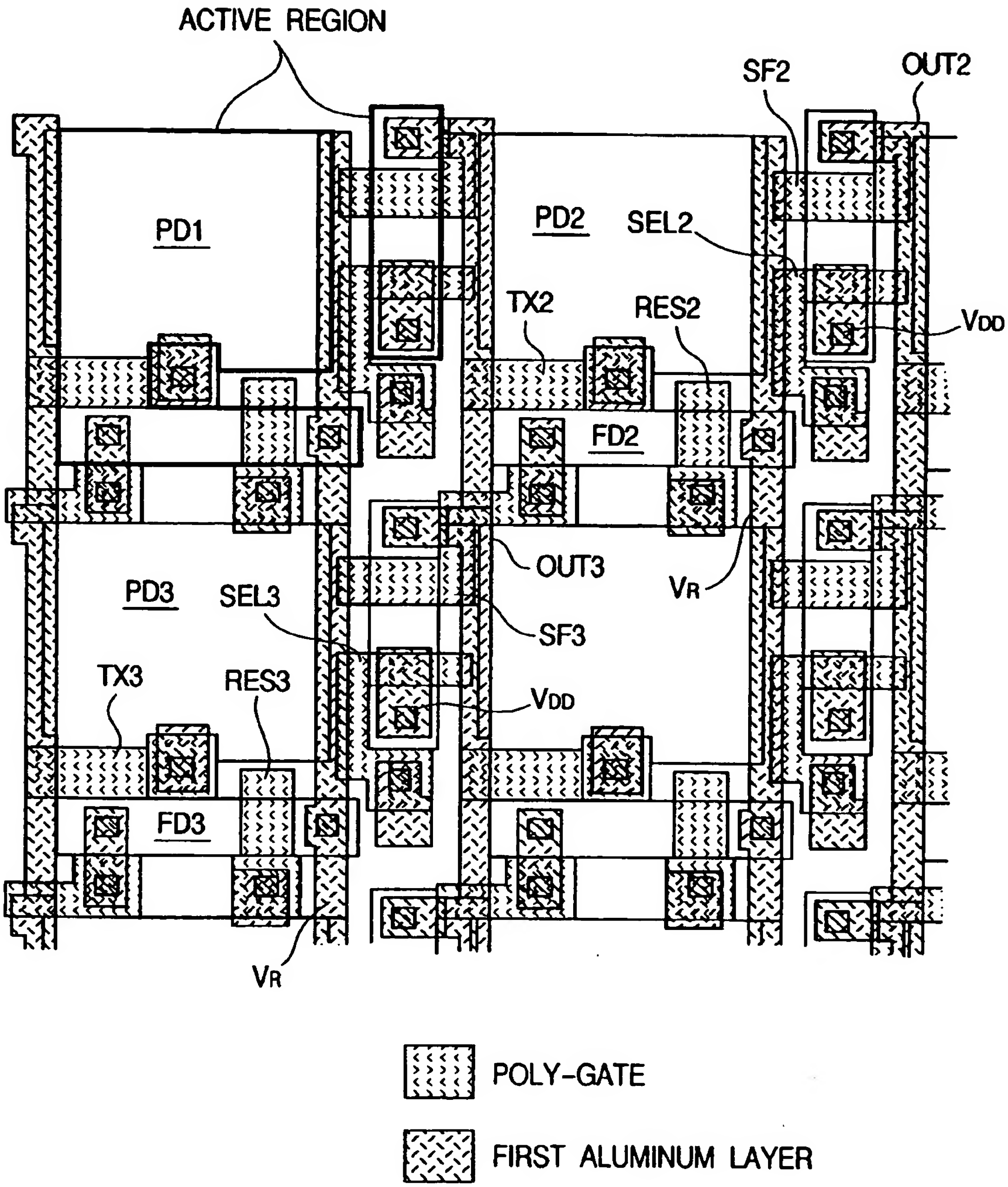
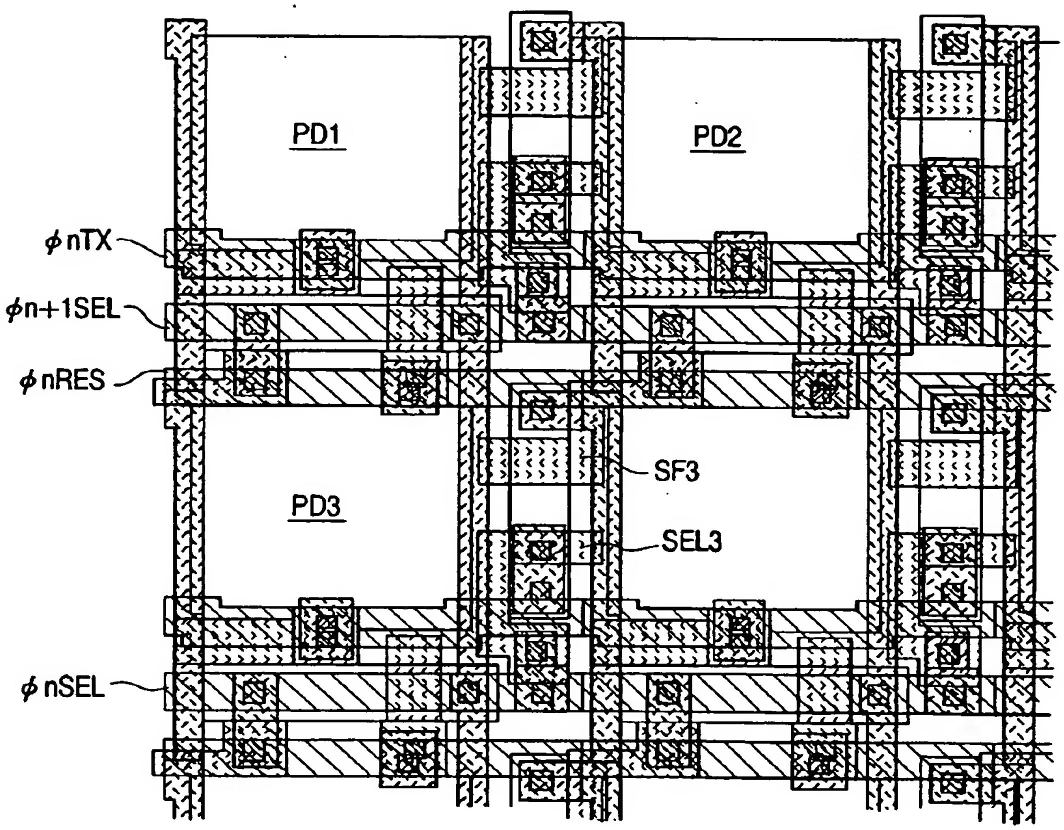

ACTIVE REGION
SF2
OUT2
PD1
PD2
SEL2
VDD
TX2
RES2
FD2
OUT3
VR
PD3
SEL3
SF3
TX3
RES3
VDD
FD3
VR
POLY-GATE
FIRST ALUMINUM LAYER

FIG. 13



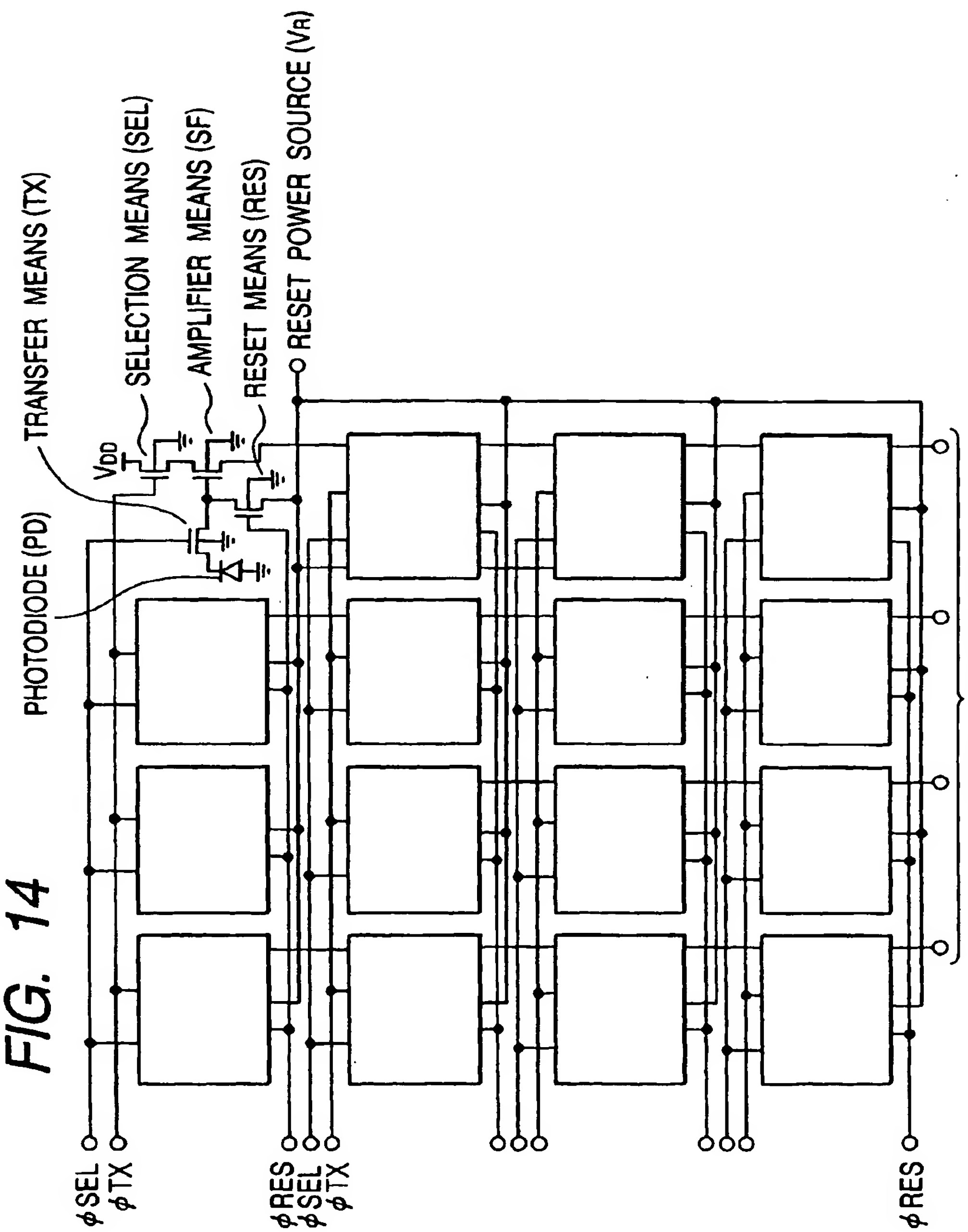

TRANSFER MEANS (TX)
SELECTION MEANS (SEL)
AMPLIFIER MEANS (SF)
RESET MEANS (RES)
RESET POWER SOURCE (VR)
VDD
PHOTODIODE (PD)
φSEL
φTX
φRES
φSEL
φTX
φRES
VERTICAL OUTPUT LINE

FIG. 14

FIG. 15

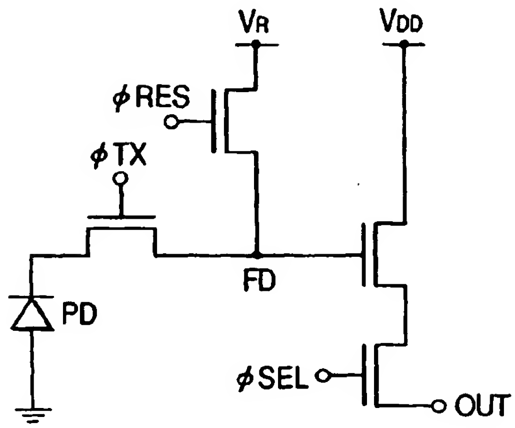

VR
VDD
ϕRES
ϕTX
FD
PD
ϕSEL
OUT

FIG. 16

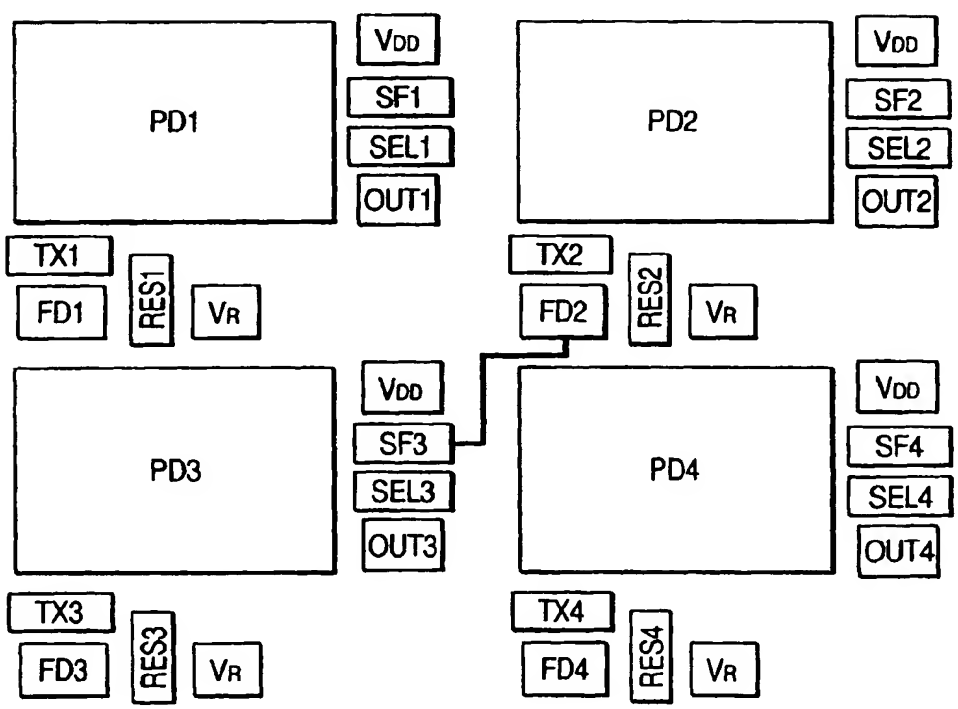
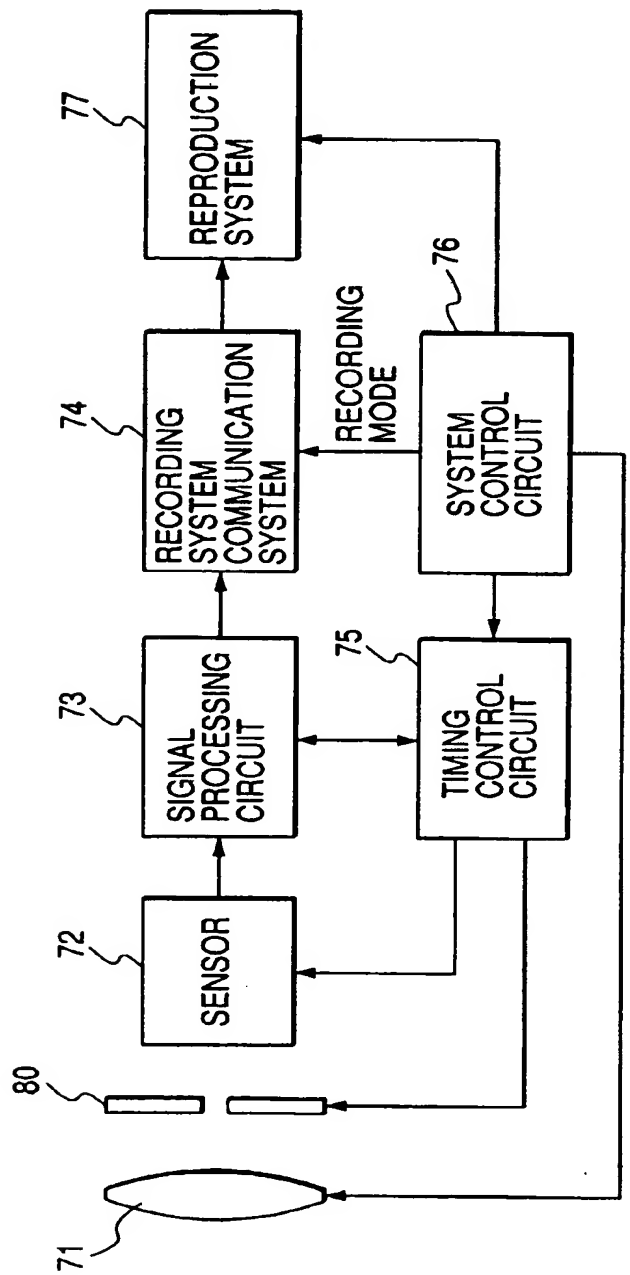

PD1
VDD
SF1
SEL1
OUT1
TX1
FD1
RES1
VR
PD2
VDD
SF2
SEL2
OUT2
TX2
FD2
RES2
VR
PD3
VDD
SF3
SEL3
OUT3
TX3
FD3
RES3
VR
PD4
VDD
SF4
SEL4
OUT4
TX4
FD4
RES4
VR

FIG. 17


71
80
72
SENSOR
73
SIGNAL PROCESSING CIRCUIT
74
RECORDING SYSTEM COMMUNICATION SYSTEM
77
REPRODUCTION SYSTEM
75
TIMING CONTROL CIRCUIT
76
SYSTEM CONTROL CIRCUIT
RECORDING MODE